REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicants thank the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-5, 7-12, and 14-22 are pending in the application. Claims 1, 8, 15, and 20 are independent. The remaining claims depend, directly or indirectly, from claims 1, 8, and 15.

Claim Amendments

Claims 1, 8, 15, and 20-22 are amended by way of this reply to clarify the scope of the invention. Claims 2-3, 7, 9-10, 14, and 16-17, which depend directly or indirectly from claims 1, 8, and 15, are amended to conform to the amendments made to claims 1, 8, and 15. No new matter has been added by way of these amendments as support can be found, for example, in paragraphs [0028] and [0037] – [0045], and Figures 2 and 4 of the originally filed specification.

Rejections under 35 U.S.C. §103

Claims 1-5, 7-12, and 14-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,510,541 ("Fujiwara") and U.S. Patent 6,009,256 ("Tseng"). To the extent that this rejection still applies to the amended claims, the rejection is respectfully traversed.

To establish a prima facie case of obviousness, "the prior art reference (or references when combined) must teach or suggest *all the claim limitations*." MPEP § 2143 (emphasis added). Further, "*all words in a claim* must be considered in judging the patentability of that claim against the prior art." MPEP § 2143.03 (emphasis added). Applicants respectfully assert that the cited

references, when combined, fail to teach or suggest all the claim limitations of amended independent claims 1, 8, 15, and 20.

Amended claim 1, requires, in part,

> removing nodes from the simulation image to produce an optimized image and an optimized nodes image, wherein the optimized nodes image comprises information about the nodes removed from the simulation image;
> simulating the optimized image; and
> when debugging is selected,
> simulating a reconstructed simulation image to gather simulation data, wherein the reconstructed simulation image comprises the optimized image and the optimized nodes image;
> debugging the simulation image using simulation data.

Claim 1 clearly requires *simulating an optimized image* produced from a simulation image and, when debugging is selected, *simulating a reconstructed simulation image* to gather simulation data, and debugging the original, un-optimized simulation image using simulation data gathered when simulating the reconstructed image. Further, claim 1 requires that the reconstructed simulation image includes the optimized image and an optimized nodes image that includes information about the nodes removed from the simulation image to produce the optimized image.

Tseng discloses a system and method in which a circuit design may be simulated in software and/or a combination of software and hardware acceleration and may also be emulated using in-circuit emulation. *See* Tseng at Abstract. More specifically, Tseng teaches that a circuit design is modeled in software models with some functionality also modeled as hardware models. *See, e.g.*, Tseng at col. 8, ll. 53-59 and Fig. 3. Further, Tseng teaches that the hardware model portion of the circuit design may be optimized to remove redundant logic and unused logic. See Tseng at col. 22, ll. 9-11. Tseng is completely silent regarding optimizing the software model portion of the circuit design. The software models are simulated in software and the hardware models are simulated by

execution on reconfigurable hardware acceleration boards. *See, e.g.*, Tseng at Fig. 3. Tseng also provides for connecting the modeled circuit design to a "target system for real environment in-circuit emulation." Tseng at col. 11, ll. 64-66. Clearly, as taught in Tseng, simulation of a modeled circuit design with software or with a combination of software and hardware acceleration is completely different from in-circuit emulation of a circuit design in a real environment.

Tseng further discloses that once a circuit design is modeled, that circuit design may be simulated in software, simulated using both software and hardware acceleration, or emulated in a target system environment. *See, e.g.*, Tseng at col. 13, l. 48 to col. 15, l. 57 and Fig. 2. In addition, information gathered while simulating the circuit design or while performing in-circuit emulation may be used to further evaluate the circuit design through further simulation of the same circuit design. *See, id.* At most, Tseng teaches *simulating* a circuit design (that may include an optimized hardware model) in software and/or with a combination of software and hardware acceleration, stopping the simulation, *emulating* the circuit design on a target system, stopping the emulation, and using the information from the emulation to further evaluate the circuit design. *See, id.*

Further, Tseng is completely silent regarding producing an optimized nodes image along with the optimized image as recited in claim 1. Because Tseng does not teach producing an optimized nodes image, Tseng cannot possibly be read to teach simulating a reconstructed simulation image that includes both the optimized image and the optimized nodes image, nor debugging the original, un-optimized simulation image using the simulation data gathered while simulating the reconstructed simulation image as also required by claim 1.

Fujiwara does not provide what Tseng lacks. Fujiwara is directed to a database for use in designing and verifying (*i.e.*, simulating) integrated circuits and a method for designing and

verifying circuits using the database. *See* Fujiwara at col. 1, l. 59 to col. 2, l. 16. Fujiwara merely discloses a general simulation procedure that uses various simulation models, including a description optimization model, and test scenarios generated from a virtual core database to produce simulation results. *See,* Fujiwara at Fig. 19, col. 15, ll. 50-55; see also, col. 1, l. 43 to col. 15, l. 49. Specifically, all Fujiwara discloses regarding performing a simulation is that "[w]hen simulation circuit conditions are input into [a virtual core database storing data for system design], a logic simulator executes simulation using pre-designed circuits for simulation and a newly-designed circuit if required, and outputs simulation results." *See,* Fujiwara at col. 15, ll. 50-55.

Further, Fujiwara teaches that the description optimization model is a model of the circuit that is optimized for simulation and is generated from an original description of a circuit *before simulation* of the circuit. *See* Fujiwara at col. 16, l. 49 – col. 19, l. 35. The optimizations disclosed by Fujiwara that may be performed on the original circuit description to create the description optimization model include removing conditional processing branches that would never be executed when simulating the circuit, performing hierarchy expansion to remove unnecessary distinctions between signal lines, removing case sentences to improve speed, and replacing portions of the circuit that will not influence simulation results with access check circuits that check for mistaken access to the removed portions during simulation. *See id.*

However, Fujiwara is completely silent regarding performing simulation in which the description optimization model of a circuit and the information removed from the original description of the circuit when creating the description optimization model are used together to "reconstruct" the original circuit description for simulation. At most, Fujiwara teaches that when hierarchy expansion is applied in creating the description optimization model, "a reference list

indicating correspondence between signal lines before and after the hierarchy expansion may be prepared, so that the original signal names before the hierarchy expansion can be used *after debugging*." Fujiwara at col. 18, ll. 14-18 (emphasis added). Thus, Fujiwara cannot possibly be read to teach simulating a reconstructed simulation image that includes both the optimized image and the optimized nodes image, nor debugging the original, un-optimized simulation image using the simulation data gathered while simulating the reconstructed simulation image as required by claim 1.

In view of the above, Tseng and Fujiwara, whether considered separately or together, do not teach or suggest all of the limitations of amended independent claim 1. Thus, claim 1 is patentable over the combination of Tseng and Fujiwara. Amended independent claims 8, 15, and 20 include at least the same patentable limitations as independent claim 1 and thus, are also patentable over the cited references for at least the same reasons. Finally, all dependent claims are patentable over the cited references for at least the same reasons as independent claims 1, 8, and 15. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicants believe this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 33226/356001; SUN040029).

Dated: August 20, 2007

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